Bilal Habib

1152 S, Thomas St, Apt 21, Arlington VA-22204, USA

C: 571-224-5978, E: <u>bhabib@gmu.edu</u>, Web: <u>http://mason.gmu.edu/~bhabib/</u>

Education

- PhD Computer Engineering, 2010-15, George Mason University, Fairfax, VA.
- MSc Computer Engineering, 2009, George Washington University, Washington, D.C.
- Bachelor of Computer Engineering, 2005, University of Engineering & Tech, Pakistan.

Research Publications

- Bilal Habib, Jens -Peter Kaps and Kris Gaj ."**Implementation of Efficient SR-Latch PUF on FPGA and SoC devices**," Journal of Computers & Electrical Engineering, 2015. (Under review).
- B.Habib, J.-P. Kaps and K.Gaj ."Efficient SR-Latch PUF," 11th International Symposium on Applied Reconfigurable Computing, 2015, Bochum, Germany, April 15-17. 2015.
- B.Habib, K.Gaj and J.-P. Kaps ."**FPGA** PUF Based on Programmable LUT Delays," Proc. 16th EUROMICRO Conference on Digital System Design, 2013, Santander, Spain, Sep. 2013.
- J.-P. Kaps, P. Yalla, K.K. Surapathi, B. Habib, S. Vadlamudi, and S. Gurung, "Lightweight Implementations of SHA-3 Finalists on FPGAs", Proc. 3rd SHA-3 Candidate Conf., Washington, D.C., Mar. 2012.
- J.-P. Kaps, P. Yalla, K.K. Surapathi, B. Habib, S. Vadlamudi, S. Gurung, and J. Pham, "Lightweight Implementations of SHA-3 candidates on **FPGAs**," Progress in Cryptology – INDOCRYPT 2011, Lecture Notes in Computer Science (LNCS), vol. 7107, Springer, Dec. 2011.

Employment History

- **Research Assistant** in the Cryptographic Engineering Research Group, George Mason University, Sep. 2010-present. Job responsibilities include,
 - Design, Development and Implementation of Cryptographic functions.
 - Efficient implementations of Low area and high throughput hardware designs.
 - Simulations with ModelSim and Isim.
 - Embedded Systems: MicroBlaze, Zynq based SoC design .
 - Python and Perl based scripting and data analysis.
 - Inter-processor communications: MPI (Message Passing Interface) based Inter processor communication protocols and implementation on hardware devices (FPGAs).
 - Design, Development, implementation and testing of Hardware primitives.
 - Hardware security.

- Physical Unclonable Functions for FPGAs.
- MSP430 micro-controllers protocols implemented: SPI, I2C, interfacing of sensors and displays. Serial and parallel interfaces.
- **Design Engineer** (Embedded Systems) at AND OR Logic Pvt Ltd, Islamabad

(http://www.andorlogic.com/) May 9, 2005 to Dec. 2007.

- Behavioral and RTL Design for Xilinx FPGAs.
- Simulation and Optimization of Verilog HDL.
- Designing Firmware for PIC and ARM Microcontrollers.
- Circuit Design and Testing.
- Board level testing, debugging and power analysis. Projects Completed:
 - Securing E1 and D1 streams with cryptographic algorithms for Radio Communication.
 - Design and Development of Tamper Proof Digital Energy Meter.

Achievements

• Ministry of Science & Technology Merit Scholarship for four consecutive years of graduate engineering studies. Sponsor www.hec.gov.pk

• Nationwide selection and then participation in International Congress, Sydney, Australia Sep. 2004, based on my essay and presentation. Sponsor www.worldenergy.org. The title of my paper was "Micro-Hydro Electric Power in Pakistan"

• Scholarship to attend a Seminar "Globalization ,Technology and Development" at San Jose State University, Jul. 14-21, 2007. Sponsored by www.theIHS.org.

• Merit Scholarships in College and School.

Software Skills

VHDL, Verilog, Assembly languages of PIC and ARM, C, C++, Java, MPI, UPC, Python, Perl, Tcl scripts.

Tools

Vivado, Xilinx ISE, Xilinx Plan Ahead, Altera Quartus, ModelSim, Matlab, MPLAB, PSPICE, Weka, Arena.

Embedded Platforms

MicroBlaze, Zynq (SoC).

Office

Microsoft Excel, Microsoft PowerPoint, Microsoft Word.

Academic Service

Reviewer Conference: CHES-(2012,13,14), DSD-(2014, 2012), ReConFIG-(2012, 13).