FARNOUD FARAHMAND

Education:

- George Mason University, Fairfax, Virginia
  PhD Computer Engineering, Expected graduation: December 2019 **GPA: 4/4**
- George Mason University, Fairfax, Virginia
  MS Computer Engineering, Sep. 2014 to Dec. 2016, **GPA: 3.83/4**
- Islamic Azad University - Tehran, Iran.
  B.Sc. Electrical Engineering, Sep. 2008 to July 2013, GPA: 3.1/4 Last two years GPA: 3.25

Working Experiences:

- **Hardware Engineering Intern** **May. 2017 – Aug. 2017**
  Google, Mountain View, CA
  Implemented power analysis flow of crypto blocks on secure micro-controller silicon projects using power estimation tools specifically for side channel analysis purposes.
  - Used Python, Tcl, Verilog and Make.
  - Worked with Primetime PX, PowerPro, NCSim and Verdi
  - Developed RTL and Gate level simulation flow in block level
  - Designed a user manual for the power analysis flow developed in this project
- Digital and analog design for electronic measurement equipment July.2012 – Oct. 2012
  Electronic Afzar Azma Company www.afzarazmaco.com/en/ , Tehran, Iran
- Providing SMART schools and houses July.2011 – Oct. 2011
  Parto negar Company, Tehran, Iran

Selected Projects:

- Developed **Minerva**, an automated and comprehensive hardware benchmarking tool written in **python**. Minerva employs a unique searching algorithm, which is customized for frequency search using CAD toolsets, in addition to support for other standard search techniques. It can incorporate an arbitrary number of predefined or user defined strategies to achieve the highest possible frequency of frequency/Area for each design.
- Implemented a testbed based on **Zynq platform** (SoC) for performance analysis of CAESAR (Competition for Authenticated Encryption) candidates and AXI Stream hardware accelerators.
  Target: Finding maximum frequency achievable by hardware accelerators experimentally on the board.
- Hardware acceleration of **Hadoop** MapReduce software framework using high-level synthesis: Svm, Naivebayes, Knn, Kmeans on **SoC (Zynq)** platform.
  Target: Reducing datacenters costs and power consumption.
- Implemented 5 **OpenCV** applications on Zynq platform using high-level synthesis.
  Target: speed up over embedded GPU and CPU implementation of corresponding **computer vision** applications alongside much lower power consumption.
- Implemented 5 round 2 SHA-3 candidates using **high-level synthesis**: Luffa, Cubehash, BMW, ECHO, Shavite.
  Target: Throughput/area result and development time comparison between RTL and HLS approach. Source codes are available at: http://cryptography.gmu.edu/athena
- High-speed implementation of 2 authenticated ciphers in RTL VHDL: AES-COPA and CLOC.
  Target: maximizing Throughput/Area, significant speed up in compare with software and low power consumption. Results available at: http://cryptography.gmu.edu
- Implemented AXI standard transaction for GMU Hardware API for authenticated ciphers.
- Designing an embedded system based on AVR microcontroller for smart homes (Hardware and Software). B.Sc. Thesis.
- Motion Sensor Alarm System based on MSP430 microcontroller: Hardware and software.

Skills:

- Programing and scripting Languages: **VHDL, Verilog, Python, Tcl, C, C++**
- Tools and Simulators: **Primetime, PowerPro**, **Synopsys DC, NCSim, Verdi, Xilinx Vivado, Xilinx ISE, Altera Quartus II, Modelsim, Active-HDL**
- HLS tool: **Vivado HLS**
- Designing and simulation of analog and digital circuits: Orcad, Multisim, Proteus
- Designing printed circuit board: Altium designer
- Microcontrollers programing tools: Code Vision AVR, Code Composer Studio
- Familiar with electrical measurement equipment: Oscilloscope, signal generator, etc.
- Hardware/Software co-design on **Zynq** platform.
- High-speed and lightweight hardware implementation (FPGA, ASIC)
- Timing analysis, AXI interface, Design Verification, Understanding of ARM architecture and AMBA protocols, NAND, DRAM and NOR memory operation, etc.

Graduate Assistantship:

- Research Assistant — Summer 2016-Spring 2017
- Lab Instructor: ECE_445 Computer Organization — Fall 2015-Spring 2016
- **Co-Instructor: ECE_699 Hardware/Software Co-design on SOCs — Spring 2016**
- Grader: ECE_511 Microprocessors — Fall 2015
- Research Assistant — Summer 2015
- Grader: IT_101 and IT_102 — Spring 2015
- Lab Instructor: Linear Control Systems Laboratory — Fall 2011
- Grader: Computer architecture — Fall 2010

Publications:

- **W. Diehl, F. Farahmand, P. Yalla, J. -P. Kaps and K. Gaj "Comparison of Hardware and Software Implementations of Selected Lightweight Block Ciphers" FPL 2017.**
- **F. Farahmand, E. Homsirikamol and K. Gaj, "A Zynq-based testbed for the experimental benchmarking of algorithms competing in cryptographic contests," 2016 International Conference on ReConFigurable Computing and FPGAs (ReConFig), Cancun, 2016, pp. 1-7.**
- E. Homsirikamol, W. Diehl, A. Ferozpuri, F. Farahmand, M. U. Sharif and K. Gaj, "A universal hardware API for authenticated ciphers," 2015 International Conference on ReConFigurable Computing and FPGAs (ReConFig), Mexico City, 2015, pp. 1-8.
- M. Malik, F. Farahmand, P. Otto, N. Akhlaghi, T. Mohsenin, S. Sikdar and H. Homayoun, "Architecture Exploration for Energy-Efficient Embedded Vision Applications: From General Purpose Processor to Domain Specific Accelerator," 2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Pittsburgh, PA, 2016, pp. 559-564.
- K. Neshatpour, A. Koohi, F. Farahmand, R. Joshi, S. Rafatirad, A. Sasan and H. Homayoun " Big Biomedical Image Processing Hardware Acceleration: a Case Study for Kmeans and Image Filtering " Invited paper at ISCAS 2016.
- E Homsirikamol, W Diehl, A Ferozpuri, F Farahmand, MU Sharif and K Gaj "GMU Hardware API for Authenticated Ciphers," Cryptology ePrint Archive July 2015.

Activities & Honors:

- **Outstanding Academic Achievement Award 2017. George Mason University**
- Member of **CERG** (Cryptographic Engineering Research Group) Since Spring 2015 http://cryptography.gmu.edu
- Member of **IAEEE** (Iranian Association of Electrical and Electronic Engineer) 2013